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| 10/671,745 | 09/29/2003 | Kazuhiro Ishiguchi | 50073-066 | 3737 |

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| EXAMINER |
|---|
| DINH, DUC Q |

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| 2629 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/671,745 | ISHIGUCHI, KAZUHIRO | |
| | Examiner | Art Unit | |
| | Duc Q. Dinh | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nose et al. (U.S Patent No. 6,819,311), hereinafter Nose, in view Kudo et al (U.S 6,781,605), hereinafter Kudo.

In reference to claim 1, Nose discloses a liquid crystal display (Fig. 11) comprising:

a liquid crystal panel (1) having a large number of picture elements arranged at intersections of plural selection lines (G1Gn) and data lines (D1-Dn);

a selection line signal output IC (11-14) for outputting a selection line signal (VG) to the selection lines (G) of said liquid crystal panel;

a signal line drive IC (20) to which an image data signal and the reference voltage are inputted, and which outputs a voltage based on the reference voltage and the image data signal to a data line of the LCD; (see Fig. 1) and

a reference voltage generator circuit (the display inherently have a voltage generating to generates the voltage VD for image DATA and BLACK voltage as shown in Fig. 1), which is arranged so as to generate a reference voltage (VD) including an

image display voltage for outputting an image write voltage (DATA) and a black display voltage for outputting a black write voltage (BLACK), switches over the reference voltage either to said image display voltage or to said black display voltage, and supplies said reference voltage to said signal line drive IC (see Figs. 1, 4, 6-9);

wherein switching said reference voltage is performed so that an image display period for supplying said image display voltage and a black display period for supplying the black display voltage are contained in one horizontal period, and the switching the reference voltage is synchronized with change in selection line signals (VGs) of lines in which an image of said selection line is written and lines in which black is written regardless of the data to be display, a voltage corresponding with a black display is applied to a signal line 3 in the black display selection period t2, and the contents of a liquid crystal 7 display a black screen, and consequently a so-called reset driving is conducted where a black display is conducted every scanning line, i.e. regardless of the data to be displayed. (see col. 8, lines 36-41).

Accordingly, Nose discloses everything except a reference voltage generator circuit, which comprises plural resistors connected in series between two voltages, generates plural reference voltages from connection points of the plural resistors, switches over the reference voltage either to an image display voltage or to a black display voltage, and outputs the switched reference voltage to plural wiring lines connected to the connection points. However, Kudo discloses a reference voltage generator circuit, which comprise a plurality of resistors connected between two voltages (VH and VL) from plurality of connecting points of the plurality of resistors, (see

Fig. 4) switches over the reference voltage either to an image display voltage or to a black display voltage (see Fig. 6) and output the switched reference voltage to plural wiring line to the connection point (see Figs. 4-6, column line 7 - col. 6 line 7).

It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the reference voltage generator circuit in the device of Nose as taught by Kudo for generating reference voltage for the data driver to avoid increase in consumption power (col. 3, lines 20-23 of Kudo).

In reference to claim 2, Nose discloses when said selection line signal output IC drives nG selection lines and a selection line clock period TH (VCLK Fig. 11) is used for driving said selection lines, a signal (OE), which makes the output of said selection line signal output IC valid when said reference voltage is switched to the image display voltage while making the output of said selection line signal output IC invalid when said reference voltage (VD) is switched to the black display voltage, is inputted to said election signal output IC during nGTH period from input of a start pulse (VST), and an inverted signal of said signal is inputted after the nGTH period (col. 14, lines 17-28).

In reference to claim 3, Nose discloses the reference voltage is switched from the black display voltage to the image display voltage at time T1 and switched from the image display voltage to the black display voltage at time T2, said selection line signal output IC outputs the selection line signals so that the lines of the selection lines

selected at time (T2-T1)/2+T1 are changed to a non-selective state at a time later than (T2-T1)/2 and earlier than T2 (see Figs 1).

In reference to claim said reference 4, Nose discloses voltage is switched in a horizontal blanking period during which no image data is loaded in said signal line drive IC (col. 3, lines 40-45).

In reference to claim 5, Nose discloses wherein said reference voltage is switched during a period when image data are loaded in said signal line drive IC (col. 8, lines 17-24).

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (U.S Patent No. 6,947,043), hereinafter Kwon, in view Kudo et al (U.S 6,781,605), hereinafter Kudo.

In reference to claim 1, Kwon discloses a liquid crystal display (Fig. 2) comprising:

a liquid crystal panel (400) having a large number of picture elements arranged at intersections of plural selection lines (G1Gn) and data lines (D1-Dm);

a selection line drive IC (300) output for outputting a selection line signal (VG) to the selection lines (G) of said liquid crystal panel;

a signal line drive IC (200) to which an image data signal and the reference voltage are inputted, and which outputs a voltage based on the reference voltage and the image data signal to a data line of the LCD; (see Fig. 1) and

a reference voltage generator circuit (the display inherently have a voltage generating to generates the voltage for normal image DATA and BLACK voltage as

shown in Fig. 3), which is arranged so as to generate a reference voltage including an image display voltage for outputting an image write voltage (DATA) and a black display voltage for outputting a black write voltage (BLACK), switches over (STV) the reference voltage either to said image display voltage or to said black display voltage, and supplies said reference voltage to said signal line drive IC (see Figs 2,3);

wherein switching (using STV signal) said reference voltage is performed so that an image display period for supplying said image display voltage and a black display period for supplying the black display voltage are contained in one horizontal period, and the switching the reference voltage is synchronized with change in selection line signals (VGs) of lines in which an image of said selection line is written and lines in which black is written regardless of the data to be display (see col. 4, lines 1-60).

Accordingly, Kwon discloses everything except a reference voltage generator circuit, which comprises plural resistors connected in series between two voltages, generates plural reference voltages from connection points of the plural resistors, switches over the reference voltage either to an image display voltage or to a black display voltage, and outputs the switched reference voltage to plural wiring lines connected to the connection points.

However, Kudo discloses a reference voltage generator circuit, which comprise a plurality of resistors connected between two voltages (VH and VL) from plurality of connecting points of the plurality of resistors, (see Fig. 4) switches over the reference voltage either to an image display voltage or to a black display voltage (see Fig. 6) and

output the switched reference voltage to plural wiring line to the connection point (see Figs. 4-6, column line 7 - col. 6 line 7).

It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the reference voltage generator circuit in the device of Kwon as taught by Kudo for generating reference voltage for the data driver to avoid increase in consumption power (col. 3, lines 20-23 of Kudo).

In reference to claim 2, Kwon discloses when said selection line signal output IC drives nG selection lines and a selection line clock period STH is used for driving said selection lines, a signal (OE), which makes the output of said selection line signal output IC valid when said reference voltage is switched to the image display voltage while making the output of said selection line signal output IC invalid when said reference voltage is switched to the black display voltage, is inputted to said election signal output IC during nGTH period from input of a start pulse (VST), and an inverted signal of said signal is inputted after the nGTH period (col. 4, lines 1-35).

In reference to claim 3, Kwon discloses the reference voltage is switched from the black display voltage to the image display voltage at time T1 and switched from the image display voltage to the black display voltage at time T2, said selection line signal output IC outputs the selection line signals so that the lines of the selection lines selected at time (T2-T1)/2+T1 are changed to a non-selective state at a time later than (T2-T1)/2 and earlier than T2 (see Figs 3; col. 4, lines 25-36).

In reference to claim said reference 4, Kwon discloses voltage is switched in a horizontal blanking period during which no image data is loaded in said signal line drive IC (col. 4, lines 46-48).

In reference to claim 5, Kwon discloses wherein said reference voltage is switched during a period when image data are loaded in said signal line drive IC (col.4, lines 31-36).

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Q. Dinh whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE can be reached on (571)272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Duc Q Dinh/
Primary Examiner, Art Unit 2629